WHAT IS CLAIMED IS:

1. A programmable controller that performs sequential processing in accordance with execution codes generated by compiling a control program, said programmable controller comprising:

a storing unit which stores the execution codes; and

a universal microprocessor which mounts an acceleration mounting unit such as a pipeline logic and cache and which is directly executed by the execution codes.

2. A control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, said control-program-development supporting apparatus comprising:

a compiler which compiles the control program into codes directly executable by a universal microprocessor that mounts acceleration mounting unit such as a pipeline logic and cache.

3. The control-program-development supporting apparatus according to claim 2 further comprising:

an optimization filtering unit which reconstructs the control program into an optimum code system by excluding not-cited variables and redundant codes and rearranging

codes for locally arranging instructions for a common input or output device is included,

wherein a control program optimized by said optimization filtering unit is newly used as the former control program.

4. The control-program-development supporting apparatus according to claim 2, further comprising:

a processing-time rough-estimating unit which has a relating table which relates a sample program having the processing time already known with the control program corresponding to the execution codes to estimate a sequential-processing execution time of a programmable controller in accordance with the relating table.

5. A control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, said control-program-development supporting apparatus comprising:

a control-program dividing unit which divides the control program into a plurality of blocks; and

a compiler which compiles all or some of the blocks into execution codes directly executable by a programmable controller.

6. The control-program-development supporting apparatus according to claim 5,

wherein the programmable controller is provided with a universal microprocessor that mounts an acceleration mounting unit such as a pipeline logic and cache.

7. The control-program-development supporting apparatus according to claim 5,

wherein the control program is a ladder diagram or an instruction list generated from the ladder diagram, and

the control-program dividing unit divides the control program into a plurality of blocks at a predetermined rung in the ladder diagram to generate a program file every block concerned.

8. The control-program-development supporting apparatus according to claim 5,

wherein the control program is a ladder diagram or an instruction list generated from the ladder diagram, and

the control-program dividing unit divides the control program into a plurality of blocks at a predetermined rung serving as a jump destination for a jump instruction in the ladder diagram to generate a program file every blocks concerned.

9. The control-program-development supporting apparatus according to claim 5,

wherein the control program is a ladder diagram or an instruction list generated from the ladder diagram, and

the control-program dividing unit extracts all or some of rungs including instructions to a common input or output device from the ladder diagram, constitutes one block of all or some of the extracted rungs, and generates a program file every blocks concerned.

10. The control-program-development supporting apparatus according to claim 5 further comprising:

an optimization filtering unit which reconstructs the control program into an optimum code system by excluding not-cited variables and redundant codes and rearranging codes for locally arranging instructions for a common input or output device is included,

wherein a control program optimized by said optimization filtering unit is newly used as the former control program.

11. The control-program-development supporting apparatus according to claim 5, further comprising:

a processing-time rough-estimating unit which has a relating table which relates a sample program having the

processing time already known with the control program corresponding to the execution codes to estimate a sequential-processing execution time of a programmable controller in accordance with the relating table.

12. A control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, said control-program-development supporting apparatus comprising:

a control-program dividing unit which divides the control program into a plurality of blocks;

a control-program converting unit which converts all or some of the blocks into advanced-language control programs described with a universal-computer-readable advanced language every blocks concerned; and

a compiler which compiles all or some of universal-computer-readable advanced programming languages corresponding every above block into directly executable codes by a programmable controller.

13. The control-program-development supporting apparatus according to claim 12,

wherein the programmable controller is provided with a universal microprocessor that mounts an acceleration

mounting unit such as a pipeline logic and cache.

14. The control-program-development supporting apparatus according to claim 12,

wherein the control program is a ladder diagram or an instruction list generated from the ladder diagram, and

the control-program dividing unit divides the control program into a plurality of blocks at a predetermined rung in the ladder diagram to generate a program file every block concerned.

15. The control-program-development supporting apparatus according to claim 12,

wherein the control program is a ladder diagram or an instruction list generated from the ladder diagram, and

the control-program dividing unit divides the control program into a plurality of blocks at a predetermined rung serving as a jump destination for a jump instruction in the ladder diagram to generate a program file every blocks concerned.

16. The control-program-development supporting apparatus according to claim 12,

wherein the control program is a ladder diagram or an instruction list generated from the ladder diagram, and

the control-program dividing unit extracts all or some of rungs including instructions to a common input or output device from the ladder diagram, constitutes one block of all or some of the extracted rungs, and generates a program file every blocks concerned.

17. The control-program-development supporting apparatus according to claim 12 further comprising:

an optimization filtering unit which reconstructs the control program into an optimum code system by excluding not-cited variables and redundant codes and rearranging codes for locally arranging instructions for a common input or output device is included,

wherein a control program optimized by said optimization filtering unit is newly used as the former control program.

18. The control-program-development supporting apparatus according to claim 12, further comprising:

a processing-time rough-estimating unit which has a relating table which relates a sample program having the processing time already known with the control program corresponding to the execution codes to estimate a sequential-processing execution time of a programmable controller in accordance with the relating table.

19. A control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, said control-program-development supporting apparatus comprising:

a control-program converting unit which converts the control program into an advanced-programming-language control program described with a universal-computer-readable advanced programming language;

a debugging-code generating unit which generates a debugging control program by inserting a line number concerned into a part corresponding to each line constituting the instruction list in source codes constituting the advanced-programming-language control program; and

a debugging executing unit which displays each line of the instruction list and the execution part of the advanced-programming-language control program by relating the former with the latter.

20. A programmable controller which performs sequential processing in accordance with execution codes generated by compiling a control program, comprising:

a first storing unit which stores the execution codes;

a second storing unit which stores the data for the

difference between an execution code stored in the first storing unit and a new execution code;

a microprocessor to be directly executed by the execution codes; and

a patch processing unit which changes an execution code currently executed to a new execution code at a predetermined timing in accordance with the difference data and continuously executing the changed execution code.

21. A programmable controller which performs sequential processing in accordance with execution codes generated by compiling a control program, said programmable controller comprising:

a storing unit which stores the execution codes; and

a microprocessor to be directly executed by the execution codes,

wherein the execution codes include binary data generated by compressing the control program.

22. A control-program-development supporting apparatus that develops a control program described with a sequential-control program such as a ladder diagram or instruction list, said control-program-development supporting apparatus comprising:

a compressing unit which compresses the control

program to generate a compressed file;

a code converting unit which generates compressed data obtained by converting the compressed file into the code system of the control program; and

a compiling unit which combines the control program with the compressed data and compiles the combined result into directly-executable codes by a programmable controller.

23. A programmable controller which performs sequential processing in accordance with a control program described with a sequential-control language such as a ladder diagram or instruction list, said programmable controller comprising:

a storing unit which stores the control program;

an instruction counting unit which counts the appearance frequency of each instruction used for the control program;

a pattern-matching-table generating unit which generates a pattern-matching table in which instructions are listed starting with the highest appearance frequency in accordance with results counted by the instruction-counting unit; and

an interpreting unit which executes the control program while pattern-matching the instructions listed in

the pattern-matching table in order and interpreting the control program into directly-executable execution codes by the programmable controller.

24. A control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, said control-program-development supporting apparatus comprising:

an instruction counting unit which counts the appearance frequency of each instruction used for the control program;

a pattern-matching-table generating unit which generates a pattern-matching table in which instructions are listed starting with the highest appearance frequency in accordance with results counted by the instruction-counting unit; and

a compiler which compiles the control program into directly executable codes by the programmable controller while pattern-matching the instructions listed in the pattern matching table in order.

25. A programmable controller that performs sequential processing in accordance with execution codes generated by compiling a control program, said programmable controller

comprising:

a storing unit which stores the execution codes;

a universal microprocessor which mounts an acceleration mounting unit such as a pipeline logic and cache and which is directly executed by the execution codes; and

a control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, which control-program-development supporting apparatus having a compiler which compiles the control program into codes directly executable by a universal microprocessor that mounts acceleration mounting unit such as a pipeline logic and cache.

26. A programmable controller that performs sequential processing in accordance with execution codes generated by compiling a control program, said programmable controller comprising:

a storing unit which stores the execution codes;

a universal microprocessor which mounts an acceleration mounting unit such as a pipeline logic and cache and which is directly executed by the execution codes; and

a control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or

instruction list, which control-program-development supporting apparatus having,

a control-program dividing unit which divides the control program into a plurality of blocks; and

a compiler which compiles all or some of the blocks into execution codes directly executable by a programmable controller.

27. A programmable controller that performs sequential processing in accordance with execution codes generated by compiling a control program, said programmable controller comprising:

a storing unit which stores the execution codes;

a universal microprocessor which mounts an acceleration mounting unit such as a pipeline logic and cache and which is directly executed by the execution codes; and

a control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, which control-program-development supporting apparatus having,

a control-program dividing unit which divides the control program into a plurality of blocks;

a control-program converting unit which converts all or some of the blocks into advanced-language control programs

described with a universal-computer-readable advanced language every blocks concerned; and

a compiler which compiles all or some of universal-computer-readable advanced programming languages corresponding every above block into directly executable codes by a programmable controller.

28. A programmable controller that performs sequential processing in accordance with execution codes generated by compiling a control program, said programmable controller comprising:

a storing unit which stores the execution codes;

a universal microprocessor which mounts an acceleration mounting unit such as a pipeline logic and cache and which is directly executed by the execution codes; and

a control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, which control-program-development supporting apparatus having,

a control-program converting unit which converts the control program into an advanced-programming-language control program described with a universal-computer-readable advanced programming language;

a debugging-code generating unit which generates a debugging control program by inserting a line number concerned into a part corresponding to each line constituting the instruction list in source codes constituting the advanced-programming-language control program; and

a debugging executing unit which displays each line of the instruction list and the execution part of the advanced-programming-language control program by relating the former with the latter.

29. A programmable controller that performs sequential processing in accordance with execution codes generated by compiling a control program, said programmable controller comprising:

a storing unit which stores the execution codes;

a universal microprocessor which mounts an acceleration mounting unit such as a pipeline logic and cache and which is directly executed by the execution codes; and

a control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, which control-program-development supporting apparatus having,

an instruction counting unit which counts the appearance frequency of each instruction used for the control

program;

a pattern-matching-table generating unit which generates a pattern-matching table in which instructions are listed starting with the highest appearance frequency in accordance with results counted by the instruction-counting unit; and

a compiler which compiles the control program into directly executable codes by the programmable controller while pattern-matching the instructions listed in the pattern matching table in order.

30. A programmable controller which performs sequential processing in accordance with execution codes generated by compiling a control program, comprising:

a first storing unit which stores the execution codes;

a second storing unit which stores the data for the difference between an execution code stored in the first storing unit and a new execution code;

a microprocessor to be directly executed by the execution codes;

a patch processing unit which changes an execution code currently executed to a new execution code at a predetermined timing in accordance with the difference data and continuously executing the changed execution code; and

a control-program-development supporting apparatus

that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, which control-program-development supporting apparatus having a compiler which compiles the control program into codes directly executable by a universal microprocessor that mounts acceleration mounting unit such as a pipeline logic and cache.

31. A programmable controller which performs sequential processing in accordance with execution codes generated by compiling a control program, said programmable controller comprising:

a storing unit which stores the execution codes;

a microprocessor to be directly executed by the execution codes,

wherein the execution codes include binary data generated by compressing the control program; and

a control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, which control-program-development supporting apparatus having a compiler which compiles the control program into codes directly executable by a universal microprocessor that mounts acceleration mounting unit such as a pipeline logic and cache.

32. A programmable controller which performs sequential processing in accordance with a control program described with a sequential-control language such as a ladder diagram or instruction list, said programmable controller comprising:

a storing unit which stores the control program;

an instruction counting unit which counts the appearance frequency of each instruction used for the control program;

a pattern-matching-table generating unit which generates a pattern-matching table in which instructions are listed starting with the highest appearance frequency in accordance with results counted by the instruction-counting unit;

an interpreting unit which executes the control program while pattern-matching the instructions listed in the pattern-matching table in order and interpreting the control program into directly-executable execution codes by the programmable controller; and

a control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, which control-program-development supporting apparatus having a compiler which compiles the control program into codes directly executable by a universal

microprocessor that mounts acceleration mounting unit such as a pipeline logic and cache.